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09/964,315	09/26/2001	Shakuntala Anjanaiah	TI-31779	9921

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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
2187	7

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,315	ANJANAIAH ET AL.	
	Examiner	Art Unit	
	Reba I. Elmore	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Specification

2. The abstract of the disclosure is objected to because of informalities:

examples are:

'have' should be –having—on line 1;

insert –a—before 'processor' in line 12.

also, 2 versions of the abstract have been provided, one version on page 22 and another version on page 23. Correction is required. See MPEP § 608.01(b).

3. The related application section on page 1 of the disclosure must be updated to show the patent application numbers for the related applications listed.

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of copending Application No. 09/964158. An analysis of claim 12 of the present invention is compared to the claims of the conflicting application. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

09/964315	***09/964158***
Claim 12	**Claim 1**
An Utopia interface unit for providing an interface between an external data processing unit and a direct memory access unit:	An ATM slave interface unit providing an interface between an ATM master processing unit and an ATM slave processing unit
	Claim 8
	the interface unit as recited in claim 1 wherein the control signals and the data cells have the UTOPIA format
	Claim 1
an input buffer memory unit for providing data cells to the direct memory interface unit	an input unit receiving data cells and exchanging control signals with the ATM master processing unit
an interface input unit for controlling the transmission of data cells from the external processing system to the input buffer memory unit	**Claim 9**
	the interface unit as recited in claim 1 wherein the ATM slave processing unit

includes a direct memory access unit

an output buffer memory unit for receiving data cells from the direct memory access unit

an interface output unit for controlling transmission of data cells from the output buffer memory unit to the external procession system

Claim 6

the interface unit as recited in claim 1 further comprising: an output buffer unit; the output buffer unit including a buffer storage unit, the buffer unit storing data cells, the output buffer unit receiving data cells from the slave processing unit, the data buffer unit exchanging control signals with the slave processing unit; and an output; the output unit receiving data cells from the output buffer unit and applying data cells to the ATM master processing unit, the output unit exchanging control signals with the output buffer unit and with the ATM master processing unit.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. Claims 1-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-17 of copending Application No. 09/964159. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

09/964315

Claim 12

An Utopia interface unit for providing an interface between an external data processing unit and a direct memory access unit:

09/964159

Claim 1

An interface unit controlling the exchange of signals between a data processing unit and a communication bus, the interface unit comprising:

	Claim 6 the interface unit as recited in claim 1 wherein the UTOPIA ATM URDATA signal corresponds to an I/O OUTDATAVALID signal, and wherein a UTOPIA ATM UXCLAV signal corresponds to an I/O INDATAVALID
	Claim 5
an input buffer memory unit for providing data cells to the direct memory interface unit	the interface unit as recited in claim 1 wherein the interface unit includes: an input interface unit; an output interface unit; an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal; and an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal
an interface input unit for controlling the transmission of data cells from the external processing system to the input buffer memory unit	
an output buffer memory unit for receiving data cells from the direct memory access unit	
an interface output unit for controlling transmission of data cells from the output buffer memory unit to the external processing system	**Claim 3** the interface unit as recited in claim 1 wherein the interface unit exchanges data groups with the direct memory access unit of the data processing unit

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1- 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sun et al.

10. Sun teaches the invention (claim 1) as claimed including a data processing system comprising:

a master-state data processing unit (e.g., see Figure 1 and col. 1, line 5 to col. 2, line 55);

a communication bus with the master-state data processing unit exchanging asynchronous transfer mode protocol signals with the bus (e.g., see Figure 1 and col. 1, line 5 to col. 2, line 55);

at least one slave-state data processing unit with the slave-state data processing unit including:

a central processing unit (e.g., see Figure 1 and col. 1, line 5 to col. 2, line 55);

a direct memory access unit coupled to the central processing unit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53);

a Utopia mode interface unit coupled to the central processing unit with the Utopia transfer mode interface unit (e.g., see Figure 1, elements 120 and 140) having:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals therewith (e.g., see Figure 1 and col. 1, line 5 to col. 2, line 55); and,

a buffer unit for buffering data signals between the direct memory access unit and the processor, wherein the transfer of data cells between the buffer memory unit and the direct memory interface unit is determined by an event signal (e.g., see Figure 1).

As to claim 2, Sun teaches the Utopia interface unit can act in a receive mode and in a transmit mode (e.g., see Figure 1, elements 120 and 140).

As to claim 3, Sun teaches the buffer memory unit is a first-in/first-out memory unit (e.g., see Figure 1, elements 120 and 140).

As to claim 4, Sun teaches an input interface unit and an output interface unit with the buffer memory unit includes:

an input buffer memory unit, wherein the transfer between the input buffer memory unit and the direct memory access unit is determined by a receive event signal (e.g., see Figure 1, elements 120 and 140 and Figure 3 and col. 4, line 25 to col. 6, line 21); and,

an output buffer memory unit, wherein the transfer between the direct memory access unit and the output buffer memory unit is determined by a transmit event signal (e.g., see Figure 1, elements 120 and 140 and Figure 3 and col. 4, line 25 to col. 6, line 21).

As to claim 5, Sun teaches data is transferred from the communication bus to the input buffer memory unit and wherein data is transferred from the output buffer memory unit to the communication unit through the output interface unit

As to claim 6, Sun teaches the input buffer memory unit and the output buffer memory units are first-in/first-out memory units

As to claim 7, Sun teaches the receive event signal is generated when the buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the buffer memory unit from the direct memory access unit is begun as signals for transmitting and receiving data using the receiving buffer and transmitting buffer which are present in the

segmentation and reassembly (SAR) integrated circuit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53).

11. Sun teaches the invention (claim 8) as claimed including a data processing system comprising:

at least one slave-state data processing unit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53);

a communication bus, the master-state data processing unit exchanging asynchronous transfer mode protocol signals with the bus (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53);

a master-state data processing unit, the master state data processing unit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53) including:

a central processing unit as being connected via the PCI bus to the SAR integrated circuit which has a memory interface (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53 and col. 6, lines 3-10);

a direct memory access unit coupled to the central processing unit (e.g., see col. 4, lines 33-47);

a Utopia interface unit coupled to the central processing unit (e.g., see col. 5, line 5 to col. 6, line 10) with the Utopia interface unit having:

a processor coupled to the communication bus and exchanging asynchronous transfer mode protocol signals therewith (e.g., see col. 5, line 5 to col. 6, line 10); and,

a buffer memory unit for buffering data signals between the direct memory access unit and processor (e.g., see col. 5, line 5 to col. 6, line 10).

As to claim 9, Sun teaches an input interface unit and an output interface unit with the buffer memory unit including an input buffer memory unit and an output buffer memory unit (e.g., see Figure 1).

As to claim 10, Sun teaches the data is transferred from the communication bus through the input interface unit to the input buffer memory unit and wherein data is transferred from the output buffer memory unit through the output interface unit to the communication bus (e.g., see Figure 1).

As to claim 11, Sun teaches the input buffer memory unit and the output buffer memory unit are first-in/first-out memory units (e.g., see Figure 1).

12. Sun teaches the invention (claim 12) as claimed including an Utopia interface unit for providing a interface between an external data processing unit and a direct memory access unit (e.g., see col. 5, line 5 to col. 6, line 10), the interface unit comprising:

an input buffer memory unit, the input buffer memory unit providing data cells to the direct memory interface unit (e.g., see col. 4, lines 33-47);

an interface input unit, the interface input unit controlling the transmission of data cells from the external processing system to the input buffer memory unit (e.g., see Figure 1);

an output buffer memory unit for receiving data cells from the direct memory access unit (e.g., see col. 4, lines 33-47); and,

an interface output unit for controlling transmission of data cells from the output buffer memory unit to the external processing system (e.g., see Figure 1).

As to claim 13, Sun teaches the input buffer memory unit and the output buffer memory unit are first-in/first-out memory units (e.g., see Figure 1).

As to claim 14, Sun teaches the first-in/first-out memory units can store at least two data cells (e.g., see Figure 1).

As to claim 15, Sun teaches data form the input buffer memory unit is transferred to the direct memory access unit in response to word-read-signal from the buffer memory unit as signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 16, Sun teaches data from the direct memory unit is stored in the output buffer memory unit in response to a word-write signal from the output buffer memory unit as signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 17, Sun teaches data is transferred from the external processing unit to the input buffer unit in response to the cell-available signal from the input buffer unit as signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 18, Sun teaches data is transferred from the output buffer memory unit to the external processing unit in response to cell-available signal form the output buffer memory unit as signals which result in read/write access to/from the buffer memories (e.g., see col. 3, lines 13-53).

As to claim 19, Sun teaches the interface unit is operating in a slave mode, the transfer of data cells form the input buffer memory unit and the direct memory access unit being determined by a receive event signal, the transfer of data cells form the direct memory access unit to the

output buffer memory unit being determined by a transmit event signal as signals for transmitting and receiving data using the receiving buffer and transmitting buffer which are present in the segmentation and reassembly (SAR) integrated circuit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53).

As to claim 20, Sun teaches the receive event signal is generated when the input buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the input buffer memory unit and the direct memory access unit is begun and wherein the transmit event signal is generated when the output buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the output buffer memory unit from the direct memory access unit is began as signals for transmitting and receiving data using the receiving buffer and transmitting buffer which are present in the segmentation and reassembly (SAR) integrated circuit (e.g., see Figure 1 and col. 2, line 65 to col. 3, line 53).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (703) 305-9706. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2187, Donald Sparks, can be reached for general questions concerning this application at (703) 308-1756. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center receptionist whose telephone number is (703) 305-3800/4700.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2187